METHODS OF MANUFACTURING INTEGRATED CIRCUIT DEVICES HAVING AN ENCAPSULATED INSULATION LAYER

Related Application

This application claims the benefit of Korean Patent Application No. 2000-74315, filed December 7, 2000, the disclosure of which is hereby incorporated herein by reference.

Field of the Invention

The present invention relates generally to integrated circuit devices and manufacturing methods therefor and, more particularly, to insulation layers that may be used to fill gaps between conductive layers and manufacturing methods therefor.

Background of the Invention

With the development of very large scale integrated (VLSI) circuits, the integration density of semiconductor devices may increase and design rules may decrease. As a result, the distance between adjacent conductive layers at the same level may decrease, which can increase aspect ratios in gaps between conductive layers.

Various technologies for filling a high aspect ratio gap between conductive layers with an insulating material have been developed. Boro-phospho-silicate glass (BPSG) and high density plasma (HDP) oxide are insulating materials that have generally good gap filling properties. Because the formation of BPSG layers typically involves the performance of a reflow process at a temperature of approximately 800°C or higher, it generally is not used in products having a design rule of 0.15 μm or less due to short channel effects of transistors. Furthermore, because HDP oxide is

generally less effective in filling gaps, it typically is not used in products having a design rule of 0.1 μm or less.

To overcome the above problems, spin on glass (SOG) may be used as a gap filling material. Because SOG is deposited in a liquid state, it may be used to fill high aspect ratio gaps between conductive layers in an effective manner. Also, because SOG has a relatively low dielectric constant and may reduce conductive coupling between adjacent conductive layers, it may be used to further increase the integration density of semiconductor devices.

While SOG liquids have generally good gap filling abilities, they are routinely densified through a curing process. During curing, a SOG layer may not be sufficiently cured at points near other layers. During a subsequent wet cleaning process, an SOG layer that is not sufficiently cured may deform due to water absorption from the cleaning solution. Furthermore, the portion of the SOG layer that is not sufficiently cured may be more readily removed due to a relatively high etch rate, which may result in profile defects. For example, in a worst case scenario, an entire SOG layer may be removed, thereby eliminating an interlayer dielectric film. Also, during subsequent thermal processing, outgassing may occur, thereby removing water from the SOG layer. This may cause, for example, via poisoning stemming from oxidation of an exposed metal wiring layer. Even if a SOG layer is successfully cured, because the etch rate of the SOG layer may be relatively high compared to other oxide layers, more serious problems may occur as a design rule decreases.

Summary of the Invention

According to embodiments of the present invention, an integrated circuit device is manufactured by forming an insulating layer on a substrate. A capping layer is formed on the insulating layer and both the capping layer and the insulating layer are patterned. Insulating spacers are formed on sidewalls of the insulating layer so that the insulating spacers, the capping layer, and the substrate enclose the insulating layer. The capping layer and the insulating spacers comprise a protective layer that may inhibit water absorption by the insulating layer and reduce the risk of profile deformation in the insulating layer. Furthermore, the protective layer may reduce outgassing from the insulating layer, which may result in via poisoning due to oxidation of a metal wiring layer.

In other embodiments, the insulating layer is a spin on glass layer and the capping layer comprises silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, and/or Al_2O_3. In still other embodiments, each of the insulating spacers has a width in a range of about 50 Å to about 200 Å.

In still other embodiments, the insulating spacers are formed by forming a second insulating layer on the capping layer, the sidewalls of the first insulating layer, and the substrate. The second insulating layer is then etched so as to expose the substrate and the capping layer.

Brief Description of the Drawings

Other features of the present invention will be more readily understood from the following detailed description of specific embodiments thereof when read in conjunction with the accompanying drawings, in which:

FIGS. 1 - 9 are cross sectional views that illustrate integrated circuit devices having encapsulated insulation layers and methods of manufacturing same in accordance with embodiments of the present invention.

Detailed Description of Preferred Embodiments

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that there is no intent to limit the invention to the particular forms disclosed, but on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the claims. Like numbers refer to like elements throughout the description of the figures. In the figures, the dimensions of layers and regions are exaggerated for clarity. It will also be understood that when an element, such as a layer, region, or substrate, is referred to as being "on" another element, it can be directly on the other element or intervening elements may be present. In contrast, when an element, such as a layer, region, or substrate, is referred to as being "directly on" another element, there are no intervening elements present. In the drawings, **FIGS. 1A** through **9A** are cross-sectional views when viewed from a direction parallel to a direction in which an active region of a semiconductor substrate used, for example, in manufacturing a DRAM extends. **FIGS. 1B** through **9B** are

cross-sectional views when viewed from a direction perpendicular to the direction in which the active region extends.

Referring to **FIGS. 1A** and **1B**, a plurality of conductive patterns **20** covered with a first insulating layer **22**, such as a silicon nitride layer, are formed on a semiconductor substrate **10** in which an active region is defined by an isolation region **12**. In accordance with embodiments of the present invention, the conductive patterns **20** may comprise a plurality of gate electrodes. A contact region **14** positioned on the active region of the semiconductor substrate **10** is exposed between each of the plurality of gate electrodes **20**. First insulating layers **22** overly the gate electrodes **20**.

Referring to **FIGS. 2A** and **2B**, a second insulating layer **30** is formed to a thickness of about 10 Å - 300 Å on the surface of the semiconductor substrate **10** exposed between the gate electrodes **20**. The second insulating layer **30** may function as an etch stop layer during subsequent processing. The second insulating layer **30** may comprise silicon nitride, silicon oxide, and/or aluminum oxide (Al_2O_3), in accordance with embodiments of the present invention. In preferred embodiments of the present invention, the second insulating layer comprises silicon nitride. In other embodiments of the present invention, the second insulating layer **30** may be omitted.

Referring to **FIGS. 3A** and **3B**, spin-on-glass (SOG) is deposited on the first and second insulating layers **22** and **30**, thereby filling a space between the gate electrodes **20**. Curing is then performed on the SOG to form a planarized SOG layer **40**.

Referring to **FIGS. 4A** and **4B**, a capping layer **42** is formed on the SOG layer **40**. The capping layer **42**, which may be removed during subsequent processing, may comprise an insulating material or a conductive material, and may be used to protect the SOG layer **40**. In accordance with embodiments of the present invention, the capping layer **42** may comprise silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, and/or Al_2O_3.

Referring to **FIGS. 5A** and **5B**, the capping layer **42** and the SOG layer **40** are patterned by photolithography using a photoresist pattern (not shown) to form a SOG pattern **40a** that exposes the first and second insulating layers **22** and **30** and a capping pattern **42a** that overlies the SOG pattern **40a**. If the second insulating layer **30** is omitted, then the contact region **14** of the semiconductor substrate **10** and the top of

the first insulating layer **22** are exposed by an opening **H** formed through the capping pattern **42a** and the SOG pattern **40a**. The SOG pattern **40a** has a first sidewall **40r** that extends vertically from the top of the first insulating layer **22** and a second sidewall **40s** that extends vertically from the surface of semiconductor substrate **10**. Conventional ashing and strip processes may then be performed to remove the photoresist pattern. Sulfuric acid may be used in a strip process, which generally does not adversely impact the profile of the SOG pattern **40a**.

Referring to **FIGS. 6A** and **6B**, insulating spacers **44** overlying the first and second sidewalls **40r** and **40s** of the SOG pattern **40a** are formed on the first and second insulating layers **22** and **30**, respectively. The width of each of the insulating spacers **44** may be about 50 Å- 500 Å. In accordance with some embodiments of the present invention, each of the insulating spacers **44** has a width of about 50 Å - 200 Å. The insulating spacers **44** may be formed by first forming a third insulating layer on the resulting structure in which the SOG pattern **40a** and the capping pattern **42a** have been formed. The third insulating layer may comprise silicon oxide, silicon nitride, undoped polysilicon, and/or Al_2O_3. The third insulating layer is then etched to leave insulating spacers **44** covering the first and second sidewalls **40r** and **40s** of the SOG pattern **40a** and the sidewall of the capping pattern **42a** on the first and second insulating layers **22** and **30**. In embodiments of the present invention in which the first insulating layer **22** comprises silicon nitride, the third insulating layer may comprise silicon oxide to allow the third insulating layer to be selectively etched with respect to the silicon nitride layer during etchback of the third insulating layer, which may minimize loss of the first insulating layer **22**.

As a result, the SOG pattern **40a** is surrounded by a protective layer, which comprises the capping pattern **42a** overlying the top of the SOG pattern **40a**, the insulating spacers **44** overlying the first and second sidewalls **40r** and **40s**, and the first and second insulating layers **22** and **30**. Together, the protective layer and the SOG pattern **40a** may comprise an interlayer dielectric pattern. If the second insulating layer **30** is omitted, then the bottom of the SOG pattern **40a** is surrounded by the semiconductor substrate **10** instead of the second insulating layer **30**.

The second insulating layer **30** may serve as an etch stop layer during etchback of the third insulating layer. Thus, the insulating spacers **44** are formed after the

etchback is complete while a portion of the second insulating layer **30** exposed by the opening **H** is substantially removed to expose the contact region **14** of the semiconductor substrate **10**. The top of the first insulating layer **22**, which is exposed by the opening **H**, may also be partially consumed. The thickness of the first insulating layer **22** may be adjusted based on the amount of material typically consumed during etchback of the third insulating layer.

Referring to **FIGS. 7A** and **7B**, a native oxide layer is removed from the contact region **14** by, for example, wet cleaning using a cleaning solution **50** or dry cleaning. If wet cleaning is used, then the cleaning solution **50** may comprise, for example, hydrofluoric acid (HF) or a standard solution (SC)-1 comprising a mixture of NH_4OH, H_2O_2, and H_2O. In accordance with embodiments of the present invention, the SOG pattern **40a** is surrounded by the protective layer, which comprises the capping pattern **42a** overlying the top of the SOG pattern **40a**, the insulating spacers **44** overlying the first and second sidewalls **40r** and **40s**, and the first and second insulating layers **22** and **30**. Thus, if the SOG pattern **40a** is not completely cured, then the protective layer may inhibit water absorption from the cleaning solution **50** and reduce the risk of profile deformation in the SOG pattern **40a** and interlayer dielectric patterns comprising the same.

Referring to **FIGS. 8A** and **8B**, after removing the native oxide layer from the contact region **14**, a conductive material, such as a doped polysilicon, is deposited on the resulting structure to fill the opening **H** with a conductive layer **60**. Because the SOG pattern **40a** is surrounded by the protective layer comprising the capping pattern **42a**, the insulating spacers **44**, and the first and second insulating layers **22** and **30**, outgassing from the SOG pattern **40a**, which may adversely impact the conductive layer **60**, may be reduced.

Referring to **FIGS. 9A** and **9B**, chemical mechanical polishing (CMP) is performed on the resulting structure in which the conductive layer **60** has been formed until the first insulating layer **22** is exposed. As a result, a portion of the conductive layer **60** is removed to thereby form a contact pad **60a**, which is self aligned by the gate electrode **20** and contacts the contact region **14**. As part of the CMP operation, the capping pattern **42a** and portions of the SOG pattern **40a** and the insulating spacers **44** are removed, and the SOG pattern **40a** is exposed on the polished surface.

The contact pad **60a** may not suffer from via poisoning caused by the SOG pattern **40a** because an interlayer dielectric pattern that comprises the SOG pattern **40a** is surrounded by the protective layer, which may inhibit outgassing from the SOG pattern **40a**.

From the foregoing it can readily be seen that, in accordance with embodiments of the present invention, an interlayer dielectric film may be formed that comprises a SOG layer that is surrounded by a protective layer. A high-density semiconductor device may be manufactured in which a contact pad is self-aligned to an underlying conductive pattern using the interlayer dielectric film comprising the SOG layer and the protective layer. During a wet cleaning step performed before forming the contact pad, but after having formed the interlayer dielectric film, water absorption and profile deformation, which may adversely affect the SOG layer, may be reduced. Moreover, the protective layer of the interlayer dielectric film may reduce outgassing from the SOG layer, which may reduce the possibility of via poisoning resulting from oxidation on the contact pad.

In concluding the detailed description, it should be noted that many variations and modifications can be made to the preferred embodiments without substantially departing from the principles of the present invention. All such variations and modifications are intended to be included herein within the scope of the present invention, as set forth in the following claims.